

# RTM Kernel Implementation on FPGA using High Level Synthesis Tool



The efficient data management is a key to the performance for many High Performance Computing (HPC) applications. The programmable devices normally support efficient utilization of data by providing a fixed architecture of caches or scratch pad memories. These caches or scratch pad memories are designed on the basis of few heuristics that are generic enough to provide varying degree of performance enhancement for various applications. However, the performance for applications having complex data accesses can still be improved by providing more customized memory layouts for those applications.

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